REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1, 2, 7, 9 through 12, and 14 through 19 are now in this case. Claims 1, 7, 11, 12, and 14 are amended. Claims 15 through 19 are added. Claims 3 through 6, 8, and 13 are canceled.

The specification is amended to correct the numerous informalities noted by the Examiner.[1] No new matter is presented by this amendment.

The drawings were objected to because of various informalities, and some drawings were objected to under 37 C.F.R. §1.84 because of reference numerals that were not present in the specification and, in the case of Figure 9, because of a double reference numeral. Amendment to Figures 1, 7C, and 9 to overcome the objections.

Regarding the objections to Figures 2, 6A, 7B, 7C (regarding reference numeral 744), and 8, the specification is amended to include the reference numerals in the drawings that were missing from the specification. Applicants respectfully submit that the insertion of the reference numerals in these locations of the specification is clearly apparent from the description and drawings as filed, and that therefore no new matter is presented by this amendment to the specification.

Regarding the objection to Figures 7B and 7C regarding what the inputs to the multiplexers are, Applicants submit that the specification is clear regarding the inputs to these multiplexers.[2] Applicants respectfully traverse the objection, to the extent of this basis. No change to the drawings on this basis is therefore presented.

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[1] Office Action of October 3, 2003, pp. 2 and 3, ¶¶ 3 through 5.

[2] *See* specification of S.N. 09/702,405, page 32, lines 24 through 28 (regarding Figure 7B); page 33, lines 6 through 10 (regarding Figure 7C).

The specification is also amended to update the serial numbers and status of the various patent applications to which reference is made, as suggested by the Examiner.[3]

Many objections to the form of the claims were made by the Examiner.[4] To the extent that the claims remain in this case, and contain the objectionable language, amendment to those claims is presented above. Applicants therefore respectfully submit that this amendment addresses each objection raised by the Examiner, and obviates the objections.

Claim 6 was rejected under §112, ¶1, as not enabled by the specification. Claim 6 is canceled, obviating its rejection.

Claim 7 was also rejected under §112, ¶ 1, as not enabled by the specification.[5] The Examiner asserted that the claim was not operable because of an informality in the claim regarding the recitation of the first and second source operands. Claim 7 is amended to overcome this and other bases of rejection, as will be described in further detail below. Applicants submit that this amendment to claim 7 also eliminates the informality regarding the source operands, obviating the rejection on this basis.

Claims 4 and 5 were rejected under §112, ¶ 2 as incomplete, due to missing elements. Claims 4 and 5 are canceled, obviating their rejection.

Claim 11 was rejected under §112, ¶2, as lacking antecedent basis for the recitation of the "CPU". Claim 11 is amended to refer instead to the microprocessor, for which proper antecedent basis is present in independent claim 1. Applicants respectfully submit that amended claim 11 is now sufficiently definite that it meets the requirements of §112, ¶2.

Claims 1, 3, 6 through 10, 12, and 13 were rejected under §103 as unpatentable over the Intel reference[6] in view of the Hennessy et al. reference[7]. Claim 11 was rejected under §103 as

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[3] Office Action, *supra*, p. 2, ¶5.
[4] Office Action, *supra*, pp. 4 and 5; ¶¶ 9 through 16.
[5] Office Action, *supra*, p. 6, ¶ 19.
[6] *IA-64 Application Developer's Architecture Guide* (Intel Corporation, May 1999).
[7] Hennessy and Patterson, *Computer Architecture – A Quantitative Approach* (2d ed., 1996)

unpatentable over the Intel and Hennessy et al. references, and further in view of the Haataja reference[8]. Claims 1 through 9 and 12 through 14 were also rejected under §103 as unpatentable over the Philips reference[9] in view of the Hennessy et al. reference.

Claim 1 is amended to overcome the rejection. The digital system of amended claim 1 now requires at least a first functional unit comprising byte intermingling circuitry that is connected to receive first and second source operands, each having an ordered plurality of fields. The byte intermingling circuitry is operable, responsive to one of a plurality of byte intermingling instructions, to place non-contiguous data from selected fields from the first source operand in a most significant portion of a destination operand, and to place non-contiguous data from selected fields from the second source operand that are at the same positions as the selected fields from the first source operand, into a least significant portion of that destination operand.

The specification clearly supports this amendment to claim 1, by reference to the examples of the PACKH4 and PACKL4 instructions.[10] Accordingly, no new matter is presented by this amendment to claim 1.

The digital system recited in amended claim 1 now has the capability of carrying out new types of byte intermingling instructions, in which data from common locations of the first and second source operands are placed into a destination operand, with the non-contiguous data from the first source operand residing in the most significant portion of the destination operand, and the non-contiguous data from the second source operand residing in the least significant portion of the destination operand. As disclosed in the specification,[11] these instructions simply the manipulation of packed data in a microprocessor by single instruction, multiple data arithmetic instructions, thus improving the overall performance of the processor.

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[8] U.S. Patent No. 6,137,836, issued October 24, 2000, to Haataja.
[9] *TM 1000 Preliminary Data Book* (Philips Electronics, 1997).
[10] Specification, *supra*, page 26, Table 9; page 30, lines 9 through 12 and lines 17 through 20.
[11] Specification, *supra*, page 24, line 23 through page 25, line 5.

Applicants respectfully submit that amended claim 1, and therefore its dependent claims, are novel and patentably distinct over the references of record in this case.

Applicants submit that the combined teachings of the references fall short of the requirements of amended claim 1. Nowhere do either of the Intel and Philips references disclose the generating of a destination operand having a most significant portion corresponding to the contents of non-contiguous data of selected fields from a first source operand and a least significant portion corresponding to the contents of non-contiguous data of selected fields from the second source operand at the same positions as the selected fields from the first source operand, as required by amended claim 1. Rather, the Intel and Philips references teach only conventional pack instructions, in which the fields from the first and second source operands are intermingled in the destination operand, or in which contiguous data are merged into the destination.[12] The Hennessy and Haataja references add no teachings in this regard.

Further, Applicants submit that there is no suggestion from the prior art to modify these teachings to provide the recited byte intermingling operation of amended claim 1. Nowhere does any of the prior art indicate that a destination operand, such as that provided by the claimed digital system, would in any way be useful in performing any sort of calculations. Only by the improper use of hindsight could one modify the teachings of these references in such a way as to reach amended claim 1.

Accordingly, Applicants respectfully submit that amended claim 1 and its remaining dependent claims are novel and patentably distinct over the prior art of record in this case.

New dependent claims 18 and 19 are added to more specifically cover aspects of Applicants' invention. Claim 18 further requires, relative to amended claim 1 upon which it depends, that the byte intermingling circuitry is operable to place most significant bytes of a plurality of fields selected from the second operand into the least significant portion of the destination operand and to place most significant bytes of a plurality of fields selected from the

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[12] *See, e.g.*, Intel, *supra*, p. 7-117 ("Mix example"); Philips, *supra*, pp. A-133 through A-137.

first operand into the most significant portion of the destination operand. Support for new claim 18 is clearly present in the specification,[13] an example of which is the disclosed PACKH4 instruction. Similarly, claim 19 further requires, relative to amended claim 1 upon which it depends, that the byte intermingling circuitry is operable to place least significant bytes of a plurality of fields selected from the second operand into the least significant portion of the destination operand and to place least significant bytes of a plurality of fields selected from the first operand into the most significant portion of the destination operand. Support for new claim 19 is also clearly present in the specification,[14] relative to the example of the PACKL4 instruction.

Applicants respectfully submit that new claims 18 and 19 are further patentably distinct over the prior art, on the grounds that the combined teachings of the references fall still further short of the requirements of the claims. Because teaching or suggestion to modify is lacking relative to amended claim 1, Applicants submit that the properly interpreted and combined prior art falls even further short of the requirements of claims 18 and 19.

Applicants therefore respectfully submit that amended claim 1 and its dependent claims are all patentably distinct over the prior art of record in this case.

Independent method claim 12 is similarly amended as claim 1, to overcome the §103 rejection. Amended claim 12 now requires the step of writing, into a most significant portion of a destination operand, non-contiguous data from selected ones of the plurality of fields from the first source operand and writing, into a least significant portion of the destination operand, non-contiguous data from selected ones of the plurality of fields from the second source operand that are at the same positions as the selected fields of the first source operand, the data being selected in accordance with a fetched byte intermingling instruction.

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[13] Specification, *supra*, page 26, Table 9; page 30, lines 9 through 12.
[14] Specification, *supra*, page 26, Table 9; page 30, lines 17 through 20.

The specification clearly supports this amendment to claim 12, again by reference to the examples of the PACKH4 and PACKL4 instructions.[15] No new matter is presented by this amendment to claim 12.

As discussed above relative to amended claim 1, the method of amended claim 12 enables new types of byte intermingling instructions that cooperate with single instruction, multiple data, arithmetic instructions performed on the intermingled data, improving the overall performance of the processor.[16]

Applicants respectfully submit that amended claim 12, and therefore its dependent claims, are novel and patentably distinct over the references of record in this case, because the combined teachings of the references fall short of the requirements of the claim. The Intel and Philips references fail to disclose the writing of a destination operand in which its most significant portion includes non-contiguous data of selected fields from a first source operand and its least significant portion includes non-contiguous data of selected fields from the second source operand at the same positions as the selected fields from the first source operand, as claimed. The teachings of the Intel and Philips references are limited to conventional pack instructions that intermingle fields from first and second source operands, or which simply merge contiguous data.[17] As noted above, the Hennessy and Haataja references add no teachings in this regard. Suggestion from the prior art to modify these teachings in order to reach the writing step of amended claim 12 is also lacking, considering that none of the prior art teaches or suggests that the forming of a destination operand as recited by the writing step of amended claim 12, would be beneficial. This leaves only the improper use of hindsight, by way of which the skilled artisan would modify the teachings of these references in such a way as to reach amended claim 12.

Accordingly, Applicants respectfully submit that amended claim 12 and its remaining dependent claims are novel and patentably distinct over the prior art of record in this case.

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[15] Specification, *supra*, page 26, Table 9; page 30, lines 9 through 12 and lines 17 through 20.
[16] Specification, *supra*, page 24, line 23 through page 25, line 5.
[17] *See, e.g.*, Intel, *supra*, p. 7-117 ("Mix example"); Philips, *supra*, pp. A-133 through A-137.

New dependent claims 15 and 16 are added to more specifically cover aspects of Applicants' invention. Claim 15 further requires, relative to amended claim 12 upon which it depends, that the writing step writes most significant bytes of a plurality of fields selected from the second source operand into the least significant portion of the destination operand, and writes most significant bytes of a plurality of fields selected from the first source operand into the most significant portion of the destination operand, as supported in the specification,[18] relative to the example of the disclosed PACKH4 instruction. Similarly, claim 16 further requires, relative to amended claim 12 upon which it depends, that the writing step writes least significant bytes of a plurality of fields selected from the second source operand into the least significant portion of the destination operand and writes least significant bytes of a plurality of fields selected from the first source operand into the most significant portion of the destination operand, as supported by the specification,[19] relative to the example of the PACKL4 instruction.

Similarly as discussed above relative to claims 18 and 19, Applicants respectfully submit that new claims 15 and 16 are further patentably distinct over the prior art, on the grounds that the combined teachings of the references fall still further short of the requirements of the claims.

Applicants therefore respectfully submit that amended claim 12 and its dependent claims are all patentably distinct over the prior art of record in this case.

Claim 7 is amended to overcome the rejection, and is now in independent form. Amended claim 7 requires that its byte intermingling circuitry is operable to place the contents of a least significant plurality of fields selected from the second source operand in a least significant portion of the destination operand and to place the contents of a most significant plurality of fields selected from the first source operand in a most significant portion of the destination operand.

The specification of this application clearly supports the amendment to claim 7.[20] An example of the operation of the byte intermingling circuitry of amended claim 7 is the disclosed

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[18] Specification, *supra*, page 26, Table 9; page 30, lines 9 through 12.
[19] Specification, *supra*, page 26, Table 9; page 30, lines 17 through 20.
[20] Specification, *supra*, page 26, Table 9; page 30, lines 13 through 16.

PACKHL2 instruction. As disclosed in the specification, this type of instruction and circuitry is particularly useful and beneficial for manipulating and preparing pairs of values to be used by packed arithmetic operations,[21] especially by providing single instruction execution techniques for so arranging these values.

Applicants respectfully submit that amended claim 7 is also patentably distinct over the prior art of record in this case. The Intel and Philips references disclose no such instruction or operation in which most significant data from one operand is placed in a most significant portion of a destination, with least significant data from another operand placed in a least significant portion of that destination. The Hennessy et al. and Haataja references add no teachings in this regard.

In addition, Applicants submit that there is no suggestion to modify the teachings of these references in such a manner as to reach amended claim 7. None of the references teach or suggest that the forming of a destination operand in the manner performed by the byte intermingling circuitry of amended claim 7, would in any way be beneficial. Only by the improper use of hindsight could one assert that a skilled artisan would modify the teachings of these references in such a way as to reach amended claim 7.

For this reason, Applicants respectfully submit that amended claim 7 is patentably distinct of the prior art of record.

New independent method claim 17 is added to more completely cover all aspects of Applicants' invention. Claim 17 corresponds to the apparatus of amended claim 7, in that it requires the step of writing into a most significant portion of a destination operand, a most significant plurality of fields selected from the first source operand and writing, into a least significant portion of the destination operand, a least significant plurality of fields selected from the second source operand. Support for this claim is readily found in the specification,[22] relative

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[21] Specification, *supra*, page 26, Table 9.
[22] Specification, *supra*, page 26, Table 9; page 30, lines 13 through 16.

to the example of the PACKHL2 instruction. The method of claim 17 provides the important benefits discussed above relative to amended claim 7.

Applicants respectfully submit that new claim 17 is also patentably distinct over the prior art of record in this case, for the same reasons as discussed above relative to amended claim 7. Nowhere do any of the references disclose the writing steps of claim 17, nor do they suggest the desirability of a destination operand constructed in such a manner. Accordingly, because the combined teachings of the references fall short of the requirements of claim 17, and because there is no suggestion in the prior art to modify those teachings so as to reach claim 17, Applicants respectfully submit that new claim 17 is also patentably distinct over the prior art of record in this case.

The references cited by the Examiner as pertinent, but that were not applied, have been considered. Applicants submit that these references fall short of the requirements of the claims now in this case.

For these reasons, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of the above-referenced application is therefore respectfully requested.

Respectfully submitted,

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37 C.F.R. 1.8

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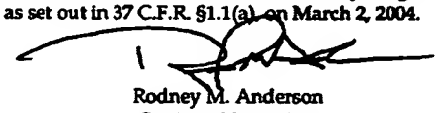

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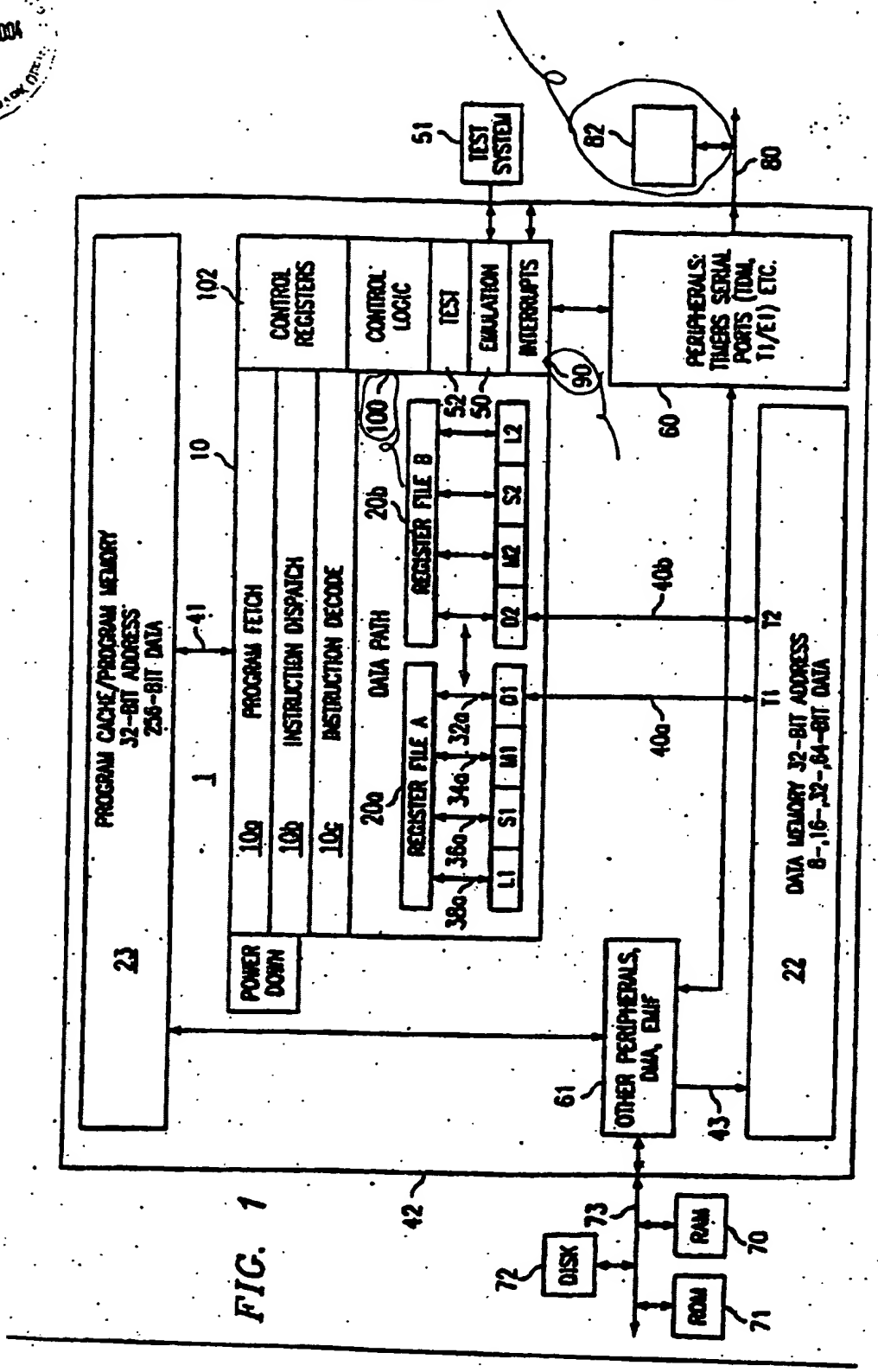

FIG. 1

ANNOTATED MARKED-UP DRAWINGS

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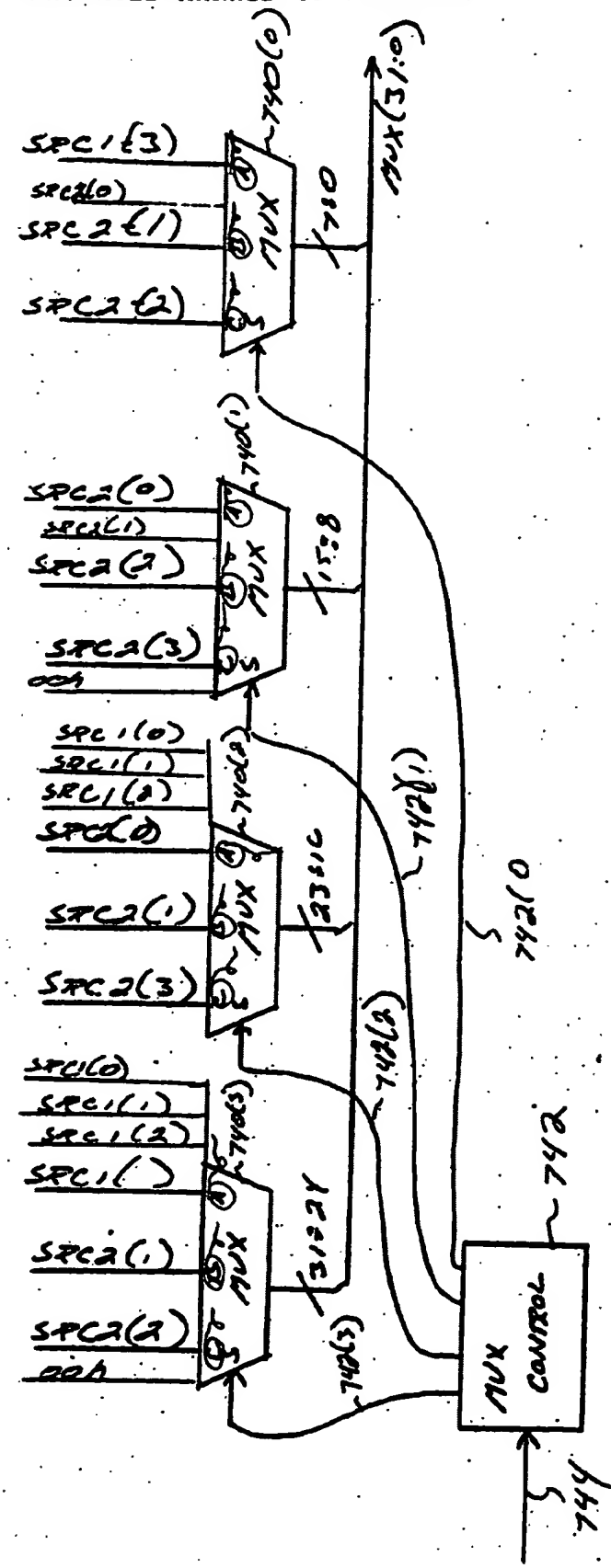

Fig. 7C

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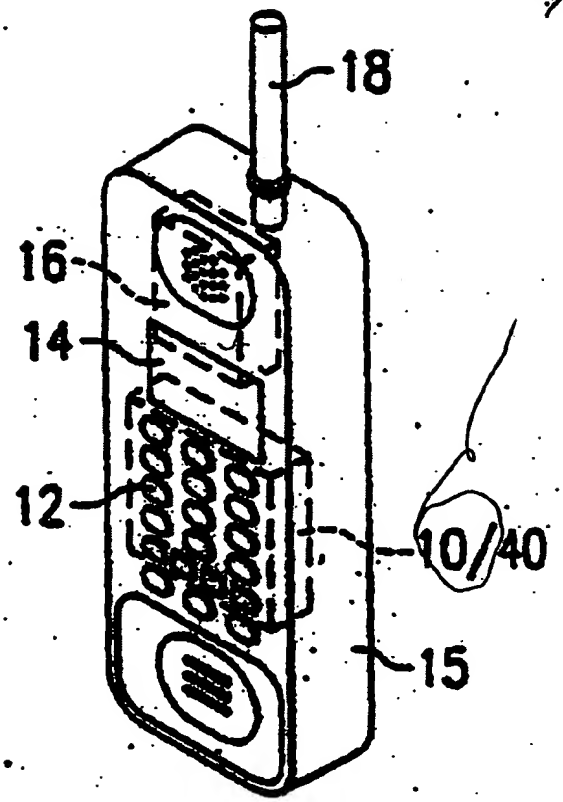

Fig 9